#4/Pre-Amdt A
4-24-02

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: : **Hidetaka NATSUME**

Filed: : **Concurrently herewith**

For: : **SEMICONDUCTOR MEMORY DEVICE.....**

Serial No. : **Concurrently herewith**

January 15, 2002

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

S I R:

Prior to the issuance of an Office Action, please amend the specification and claims as follows:

IN THE CLAIMS:

Please amend the following claims with the following:

3.(Amended) A semiconductor memory device according to Claim 1, wherein:

said second electrical conductor is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection A, the gate electrode being in common to said first driver transistor; and

a first interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said third interconnection is in contact with